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10/785,645	02/24/2004	Hartmut B. Brinkhus	VBW 5635	2374

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SENNIGER POWERS
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EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
06/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspatents@senniger.com

Office Action Summary	Application No.	Applicant(s)	
	10/785,645	BRINKHUS, HARTMUT B.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-11 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-11 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119(a)-(d) as follows: Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a certified English translation of the foreign application must be submitted in reply to this action. 37 CFR 41.154(b) and 41.202(e).

Failure to provide a certified translation may result in no benefit being accorded for the non-English application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5-11, 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schloterer et al U.S. Patent No: 5,751,234 **[herein after Schloterer]** and further in view of Quatse et al, U.S. Patent No: 4,774,656 **[herein after Quatse]**.

1. **As per Claim 1**, Schloterer teaches an interface circuit **[Col. 1, Lines 20-29, "Integrated Circuit"]** for process connections to computer, the interface circuit comprising:

(a) At least one bidirectional input connection **[Fig. 2, element 52, "Port A" – Also see Col. 23, Lines 4-5]**

(b) At least one bidirectional output connection **[Fig. 2, element 54, "Port B" – Also see Col 23, Lines 53-55]**, said bidirectional output connection connecting the interface circuit to a logic circuit **[Fig. 2, Element 30, "Microprocessor"]**

(c) Plurality of switches **[Fig. 3, Elements 108, 110, 112]** whose inputs are connected directly or indirectly to said at least one bidirectional input connection **[see Fig. 2, *elements 62 and 64 whose representation is shown in detail in Fig 3 is connected to I/O Ports A, B and C via "Data & Control Bus"*]** and having a control pin for receiving first control signals **[see Col. 7, Lines 42-46]**.

(d) Plurality of multiplexers **[Fig. 3, Elements 102, 104, 106]**, whose inputs are connected to outputs of said switches **[see Fig. 3, element 68 – output of the switches (i.e. 108-112) is connected to element 68 of the MUX]** and having control pins for receiving second control signals, which can be controlled by signals **[see Col. 7, lines 42-47 – it is inherent that a MUX would have a control pin configured to receive a signal to control the switch path]**.

(e) At least one analog comparator **[Fig. 2, elements 50 and 58]** whose input is connected to an output of one of said multiplexers **[see Fig. 36, elements 66, 68 ('MUXES') & element 58 – output of the MUXES is effectively connected to the input of the Comparators (element 58)]**

(f) At least one digital/analog converter **[Col. 56, Lines 40-42]** whose input is connected to an output of one of said multiplexers **[see Fig. 36, output of element 66, 68 (MUXES) connects to the A/D converter element 78]**

(g) Wherein according to the state of one or more of the first and second signals which control the switches and multiplexers **[Col. 38, Lines 29-30, *"Signal SAMPh which controls the sample and hold switches 108, 110 and 112"*]** the switches, multiplexers, analog comparators and digital/analog converters are activated, deactivated, or changeable into different operating or switching states, with different analog or digital functions being assignable to the one or more bidirectional input connection **[Col. 34, Lines 35-39]**

Schloterer teaches the above limitations, however fails to teach a system wherein the output port is connected to the logic circuit (microprocessor) by a galvanic decoupling device. Quatse teaches a system wherein the Central Unit is connected to an interface circuit by way of a galvanic decoupling device **[see Quatse, Col. 2, Lines 16-29]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Schloterer with that of Quatse in order to insure that input/output circuits in

which the inputs and outputs channels are suitably isolated from the bus conductors of the central unit so as to protect the central unit against any disturbance occurring in the connecting strip **[see Quatse, Col. 1, Lines 56-64]**. It is for this above stated reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings of Schloterer and Quatse.

2. **As per Claim 3**, Schloterer as modified by Quatse teaches an interface circuit wherein the multiplexers can be operated bidirectional **[see Schloterer, Col. 7, Lines 42-46]**

3. **As per Claim 5**, Schloterer as modified by Quatse teaches an interface circuit wherein the one or more analog comparators are associated with a sample-and-hold circuit, whose input is connected to at least one input connection **[see Schloterer Col. 38, Lines 26-28]**.

4. **As per Claim 6**, Schloterer as modified by Quatse teaches an interface circuit wherein the one or more analog/digital converters operate according to the principle of successive approximation **[see Schloterer Col. 56, Lines 40-42, *'The A/D converter is an eight bit successive approximation A/D converter.'*]**

5. **As per Claim 7**, Schloterer as modified by Quatse teaches an interface circuit wherein between the one or more input connections are one or more analog comparators, a current/voltage converter is connected with the connection being switchable by the multiplexer **[see Schloterer Col. 1, Lines 41-48]**.

6. **As per Claim 8**, Schloterer as modified by Quatse teaches an interface circuit wherein one or more of the analog comparators are connected after the controllable hysteretic circuit **[see Schloterer Fig. 2, elements 50 and 58]**.

7. **As per Claim 9**, Schloterer as modified by Quatse teaches an interface circuit wherein a digital/analog converter is connected in the signal direction from the output connection to one or more input connections, with the connection being switchable in a controlled way by the multiplexer **[see Schloterer Col. 7, Lines 34-46]**.

8. **As per Claim 10**, Schloterer as modified by Quatse teaches an interface circuit, wherein at least two input connections are connected to each other over a measurement resistor and a controllable switch, with both connections of the measurement resistor being connected to a differential amplifier,

whose output is connected to one or more analog/digital converters **[see Schloterer Fig. 3, elements 84 and 80].**

9. **As per Claim 11 and 13**, Schloterer as modified by Quatse teaches an interface wherein several interface circuits are connected in a cascade arrangement and connected to the logic circuit **[see Schloterer Fig. 1, element 12]**

10. **As per Claim 14 and 15**, Schloterer as modified by Quatse teaches an interface wherein a decoupling device is connected between the interface circuit and the logic circuit **[see Schloterer Fig. 3, element 90]**

11. **As per Claim 16**, Schloterer as modified by Quatse teaches an interface circuit wherein higher functions are implemented in the logic circuit **[see Schloterer Col, 13, Lines 55-59]**, while only functions are implemented in the interface circuit **[see Schloterer Col. 1, Lines 21-29]**.

12. **As per Claim 17**, Schloterer as modified by Quatse teaches an interface circuit wherein the higher functions comprise system functions **[see Schloterer Col, 13, Lines 55-59]**.

13. **As per Claim 18 and 19**, Schloterer as modified by Quatse teaches an interface circuit wherein the logic circuit and the interface circuit are configured such that bidirectional serial communication takes place between these circuits **[see Schloterer Col. 10, Lines 18-23]**

Response to Arguments

14. Applicant's arguments filed 03/20/2007 have been fully considered but they are not persuasive. First and foremost, most of Applicant's arguments were directed to the newly amended matter of the claims and thus proper citations have been addressed above in view of the said amendments. The arguments not directed to new matter, Applicant argues that prior art fails to disclose or suggest the express requirement of (a) both an analog comparator and a digital/analog converter whose inputs are connected to outputs of a multiplexer, whose input is connected to output of a switch, whose input is connected to a bidirectional input connection which is connected to a logic circuit (b) switches, multiplexers, analog comparators, and digital/analog converters are activated, deactivated, or changeable with different analog or digital functions being assignable to the one of more bidirectional input connections.

15. With respect to Argument (a). **Examiner disagrees**. For the benefit of the Applicant, Examiner would like to draw attention to Schlotterer Fig. 36 to show the alleged deficiency in prior art. Schlotterer teaches a system having a comparator subsystem (which further includes multiple comparators) **[Fig. 36, element 58]** and Analog/Digital Converter **[see Fig. 36, element 78]** whose inputs are functionally connected to a switch (within the MUX) **[see Fig. 36, elements 66,68]**. Furthermore, as can be seen in Fig. 2 – the bidirectional Ports A & C **(elements 52 & 56)** are connected to the MUX by way of Data and control bus **(element 34)**.

16. With respect to Argument (b). **Examiner disagrees**. Schlotterer teaches a system wherein the above-mentioned devices can be either activated, deactivated or state changed by way of analog or digital functions. Without having to rely on any reference, it should be inherent to the Applicant and to one of ordinary skill in the art that devices such as switches and multiplexers would need to be controlled by some signal (either analog or digital) in order for them to decide between which state to selection to make. However, regardless of that fact, Schlotterer clearly teaches in **Col. 38, Lines 25-31** where in a digital signal (ADCR[1] bit) is used to control the three sample and hold switches 108, 110 and 112. Furthermore, Schlotterer in Fig. 25 teaches having three separate signals "DISABLE, SELh and PH2b" that control the other I/O devices. Schlotterer in Col. 34, Lines 35-39 teaches the "**DISABLE signal** corresponds to the microprocessor's IO OFF signal, **used to disable all I/O devices**..."

17. Therefore in view of above response, Examiner submits that the prior art of record still reads on the amended and argued claims and therefore they stand rejected as addressed above.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
5/23/07

KIM HUYNH
SUPERVISORY PATENT EXAMINER
5/29/07